Effective Way of Conducting Highly Accelerated Life Testing – Linking the Failure Mode Effects Analysis and Finite Element Analysis

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Abstract

In today's competitive marketplace, the design phase presents a perfect opportunity to test a product to find its maximum limitations and weak links. On the same context HALT (Highly Accelerated Life Test) has been adopted by many industries. HALT is a destructive stress testing methodology for accelerating product reliability during the engineering development process. It is a great process used for precipitating failure mechanisms in an electronics hardware design and product which may occur into the field.
The traditional HALT process which is followed by most of the industries, deals with destructive stress testing and subjective approach to fix the design weaknesses based on experience, followed by iterative HALT to check the robustness against the design fixes done which may not be relevant fixes.
This paper summarizes the effective way of conducting HALT by emphasizes on the "Analysis First" approach, the FMEA (Failure Mode Effect Analysis) and FEA (Finite Element Analysis) which will help identifying the critical functions along with associated components to be monitored during HALT and reduces the iteration of HALT by analyzing the board robustness against the stresses i.e. temperature and vibration prior to HALT respectively. And also presents the specification limits derived based on the product specification and chamber standard deviation, up to which the root cause and design fixes needs to be done, eliminating the subjectivity around it.
Keywords: HALT, FMEA, FEA

I. Introduction

HALT (Highly Accelerated Life Testing) is a qualitative approach to identify the design weaknesses and improve on the design margins of the electronics assemblies. Extensive studies have been done to understand the HALT methodology and its benefits by many industries. Conducting conventional HALT requires a detailed plan with understanding of applicable stress profiles, functional test, cross functional team responsibilities [1]. This paper will explain in brief the effective HALT methodology including the FMEA and FEA activities prior to HALT to reduce design iteration and also derive specification limits [2] for the root cause analysis. The placements of thermocouple and accelerometer have also been discussed to take a decision for design fixes.

HALT tests methods are developed to find design defects and weaknesses in electronic and electromechanical assemblies so that a more reliable product can be released to market in rapid order. The product specification always can be defined as per the Figure 1 below which shows how the product can be used in unknown environment (red in color).

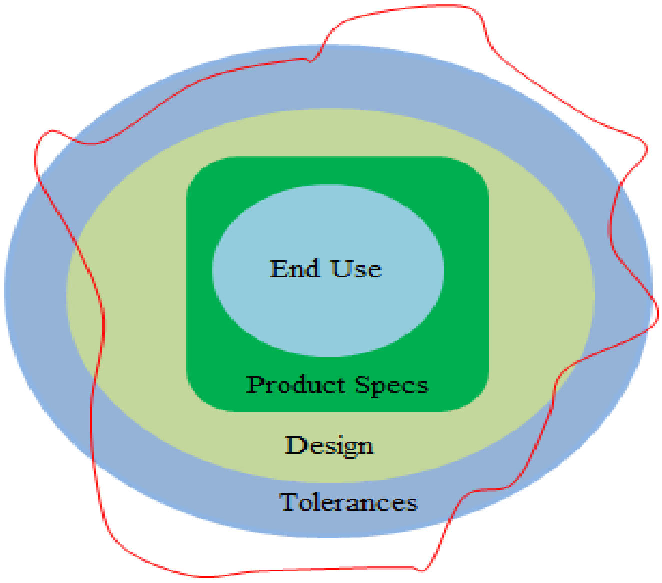

Figure 1: *Product Specifications & Field Environment*

Based on the field profile and applicable stress study, the engineered systems deliver stresses of temperature, rapid thermal cycling, and random, tri-axial vibration which are used to rapidly reveal design weaknesses in electronics and electromechanical product assemblies. Hence the conventional HALT is performed considering the sequence of stresses as follows:

- Thermal Cold Step Stress
- Thermal Hot Step Stress
- Rapid Thermal Transition Cycling
- Vibration Step Stress
- Combined Environment (Thermal Transition Cycling and Vibration Step Stress)

Traditionally in the HALT process, product design/material limitations may be discovered for each stress that is applied. Each of these limitations should have their root-cause understood and corrective action implemented based on product specification. The specification limits for doing the RCA (Root Cause Analysis) for all issues which should be corrected are subjective in nature.

The process of conventional HALT and proposed effective way of conducting HALT is explained in below paragraphs with their limitation and advantages respectively.

II. Conventional HALT Methodology

The conventional HALT methodology deals with the five different stress profiles as mentioned above. The detail test is conducted based on the profiles with limited inputs from the FMEA and FEA. The conventional HALT process is depicted in the below Figure 2.

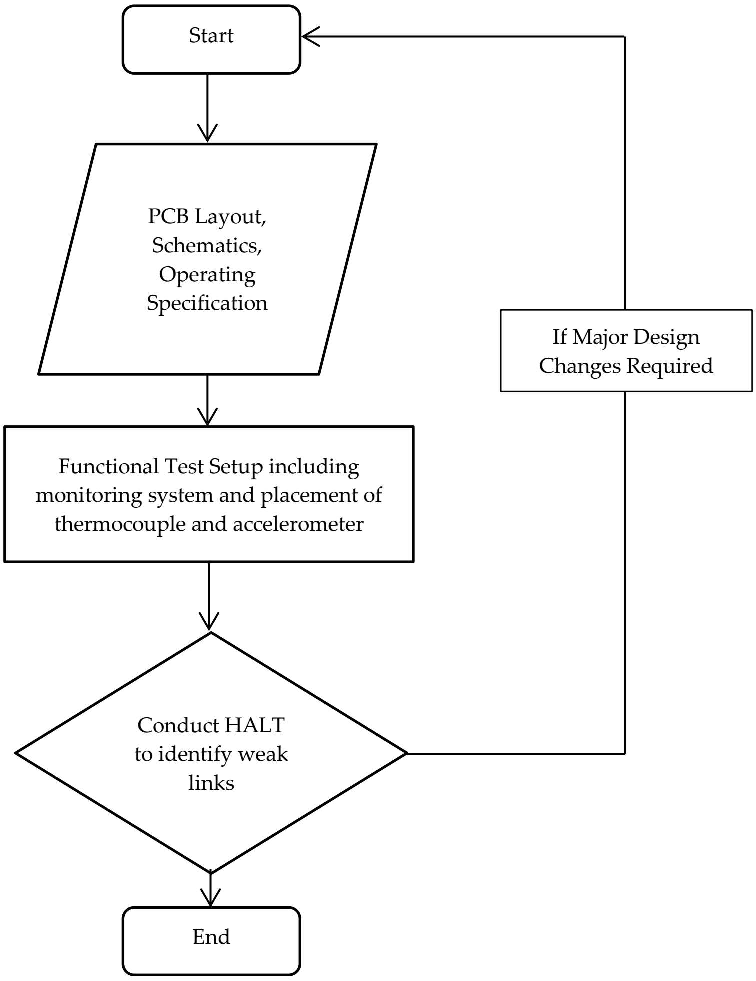

Figure 2: *Conventional HALT Methodology*

III. Proposed Effective HALT Methodology

The effective HALT methodology incorporates inclusion of FMEA outputs for identification of critical components and functions to be monitored along with FEA to validate the PCB design against the temperature cycling and the random vibration stresses prior to testing. This approach helps to identify the weak links in the design through analysis and reduces the iteration of HALT.
The advantages of Effective HALT are as follows:

- The inclusion of FMEA helps in identification of critical function which needs to be monitored during HALT and hence cross verify the performance of all the component as per the functional requirement and its criticality ranking.
- Inclusion of FEA helps in identification of design flaws prior to HALT and reduce the design iteration post HALT.
- Placement of thermocouple and accelerometer can be identified based on the FEA results i.e. most heat dissipating component and most resonant component respectively.
- Identification of specification limit helps in taking decisions for RCA needs to be done and

with its limits.

- The effective HALT helps in identification of weak links and improve the design robustness by involving cross functional team inputs and recommendations.

In the process of doing FMEA and FEA there may be chances of getting multiple number of functions and component which needs to monitored during HALT. The functional test of associated component along with the placement of thermocouple and accelerometer can be finalized by doing tradeoff between the severity ranking (can be rated in scale of 1 to 10) for the functions in FMEA and occurrence ranking (can be rated in scale of 1 to 10) for the identified stressed component in FEA. The proposed approach enables to identify the functions to be monitored and component based on the tradeoff on severity*occurrence rating.

The flow chart shown in Figure 3 summarizes the steps to conduct HALT effectively with brief explanation of key activities.

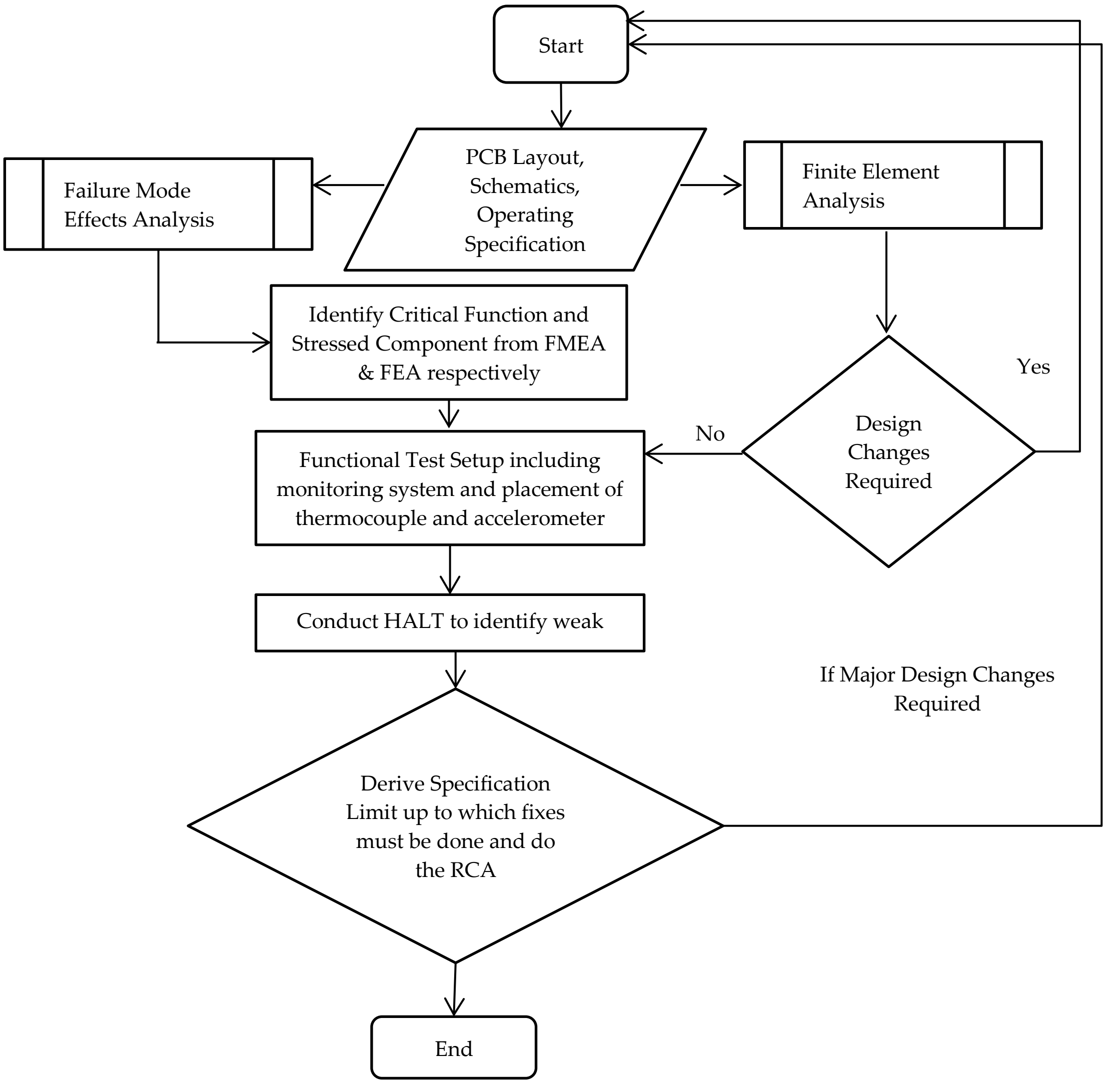

Figure 3: *Effective HALT Methodology*

I. Failure Mode Effect Analysis

The main objective of Failure Mode Effect Analysis (FMEA) is to thoroughly analyzes product design against all failure modes and reduce the associated risks. During each stress profile, functional testing is performed on the product sample to evaluate its operation performance. To verify the functionality of the board the FMEA is best way to identify the safety or mission critical functions and the respective associated failure mode of the components. For conducting effective HALT this exercise helps in identification of critical functions of the product which needs to be monitored during HALT and respective components. The functional test setup during the HALT should be made such that it covers all the critical functionalities of the product.

II. Finite Element Analysis

Finite Element Analysis (FEA) as applied in engineering is a computational tool for performing engineering analysis. This analysis is carried out for electronic and electromechanical assemblies to verify its performance against the temperature and vibration profile. These exercises help on identification of the stressed components and also design flows, if any prior to HALT to reduce the HALT iteration. The placement of thermocouples and accelerometers also becomes very important. The outputs of both needs to be analyzed to take a decision for the fixes. So the placement of thermocouple and accelerometer is also needs to be done based on the stressed component identified during the analysis.

III. Specification Limits

After conducting HALT two concerns always arise. The first is: which issues should be corrected; and the second is: should all issues be corrected? To resolve this issues in HALT the operating limits are considered, and the specification limits are derived for which the root cause analysis must be done, considering the components specification and operational limits with ±3σ range [3]. An example is shown in below Table 1 to derive the specification limits considering 2°C & 2 Grms as standard deviation for the thermocouple and accelerometer reading respectively.

Table 1: *Specification Limits Calculation*

S. No.	Factors	Values
1	Hot Temperature Specification	85°C
2	Hot Temperature Operating Limit	98°C
3	Proposed Hot Temperature Specification Limit	98°C + 6°C (i.e. 3*(σ)) = 104°C
4	Cold Temperature Specification	-40°C
5	Cold Temperature Operating Limit	-54°C
6	Proposed Cold Temperature Specification Limit	-54°C +(-6°C) (i.e. 3*(σ)) = -60°C
7	Vibration Specification	2.24 Grms
8	Vibration Operating Limit	5 Grms
9	Proposed Vibration Specification Limit	5 Grms +(6 Grms) (i.e. 3*(σ)) = 11 Grms

The above derived specification limits are shown in graphical form in the below Figure 4.

Temperature

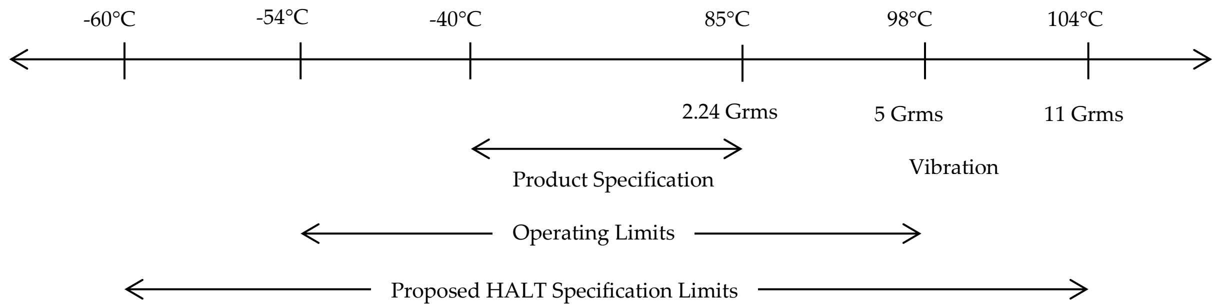

Figure 4: *Proposed HALT Specification Limits*

III. Conclusions

In this paper effective way of conducting HALT is explained in detail. Inclusion of FMEA and FEA with specification limits up to which RCA needs to be conducted are mentioned with the respective advantages. The above mentioned way of conducting HALT helps in identifying the weak links more accurately and reduce the iteration of HALT also the design.

References

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