# McCMOS Based Low Power and High Speed 32 x 32 Bit Nikhilum Multiplier

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**Abstract**

*Leakage power is the significant component of total power dissipation in nano-scale devices. Leakage power is inversely proportional of channel length. So as the device dimensions are reduced, to incorporate more no of devices, for more function to be performed, subthreshold leakage current & hence leakage power will increases. To reduce the leakage power, channel length has to be increased. So we use non-minimum length transistors to reduce the leakage current thus power. This technique is called Multiple Channel CMOS (McCMOS). Vedic mathematics is the branch of mathematics which depends upon 16 sutra and 13 up-sutra, given between 1911 and 1918 by Sri Bharati Krisna Tirthaji (1884-1960). In this paper we had used McCMOS technique as well as ancient Vedic technique Nikhilum Sutra to reduce the power dissipation and increase the speed of the multiplier. The designed 32 x 32 bit multiplier dissipates a power of 0.556 mW and a propagation delay of 27.82 nsec. 60510 transistors were used in this design. These results are improvements over power dissipations and delays reported in literature for Vedic and Booth Multiplier.*

**Keywords:** McCMOS, Vedic Mathematics, CMOS, Leakage current, Urdhva Tiryakbhyam, Nikhilum Sutra, Leakage Power consumption.

## **1.** Introduction:

In order to increase the functionality of any IC, more no of devices are embedded on the same chip. For this individual transistor has to be occupied less area. Hence their dimension has to be decreased. But at same time, Leakage current and leakage power will increases, as these are inversely proportional to the channel length. So there is a compromise. If we want to increase the functionality of the chip we need to embed more no of devices. To embed more no of devices in the same area of chip, we need to scale down the dimension of individual devices. But for nano scale devices, second order effects like DIBL are more pronounced. Hence subthreshold current and power will be more in these devices. To reduce the power we have to increase the channel length. So we use NMOS as increased channel length to control the subthreshold current. Pmos are made with smaller channel length devices. In Vedic mathematics, Nikhilum Sutra, is the method to produce the calculation in less time. Let us discuss these two methods in details.

## **1.1** McCMOS Technique

We designed a McCMOS inverter and other basic building block. In this all NMOS are made with a channel length of 29 nm and all PMOS are made with 16.5 nm. These data are taken by repeatedly choosing different length and measuring power delay product. The channel length of the PMOSs are taken 0.5 nm higher than the 16nm technology to incorporate the lateral diffusion. The effect of channel length on threshold voltage (and leakage) is very well documented

demonstrating that $V_{TH}$ decreases rapidly as effective channel length ($L_{EFF}$) is reduced [10].

First we optimize the basic gates using McCMOS technique. Fig 1 shows the design of inverter using CMOS, whereas fig 2 shows the inverter circuit using McCMOS technique. Table 1 shows power delay product difference in CMOS inverter and McCMOS inverter. Table 2 shows how we arrive to the specific length & width of the transistor used in McCMOS technique.

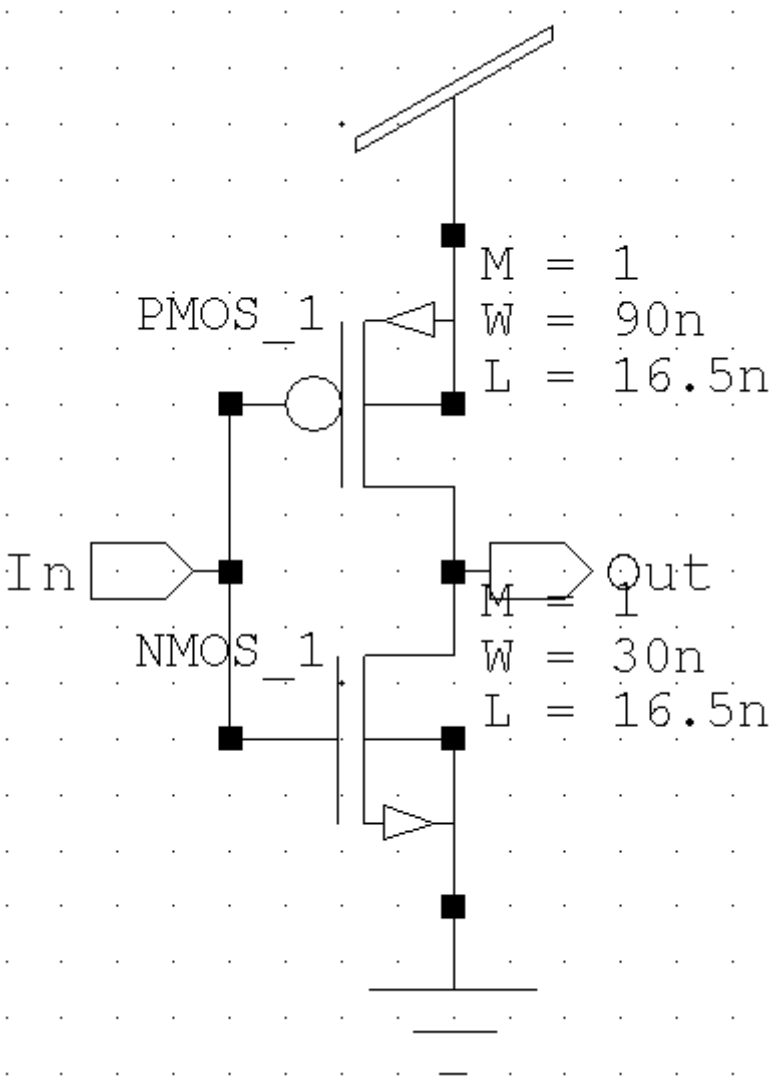


Fig 1: CMOS inverter circuit using 16nm technology

From table 1.1 & 1.2 it is clear that McCMOS inverter design with NMOS W=29n L=29n PMOS W=99n L=16.5n is best as far as PDP is concern.

**Table 1.1: Comparison of power delay product of CMOS & McCMOS inverter**

| Technique | W & L | Power (nW) | Delay (nsec) | PDP ( nW-nsec) |
|---|---|---|---|---|
| CMOS | **NMOS** W=30n L=16.5n<br>**PMOS** W=90n L=16.5n | 45.4 | 0.294 | 13.3 |
| McCMOS | **NMOS** W=29n L=29n<br>**PMOS** W=99n L=16.5n | 42.4 | 0.286 | 12.1 |

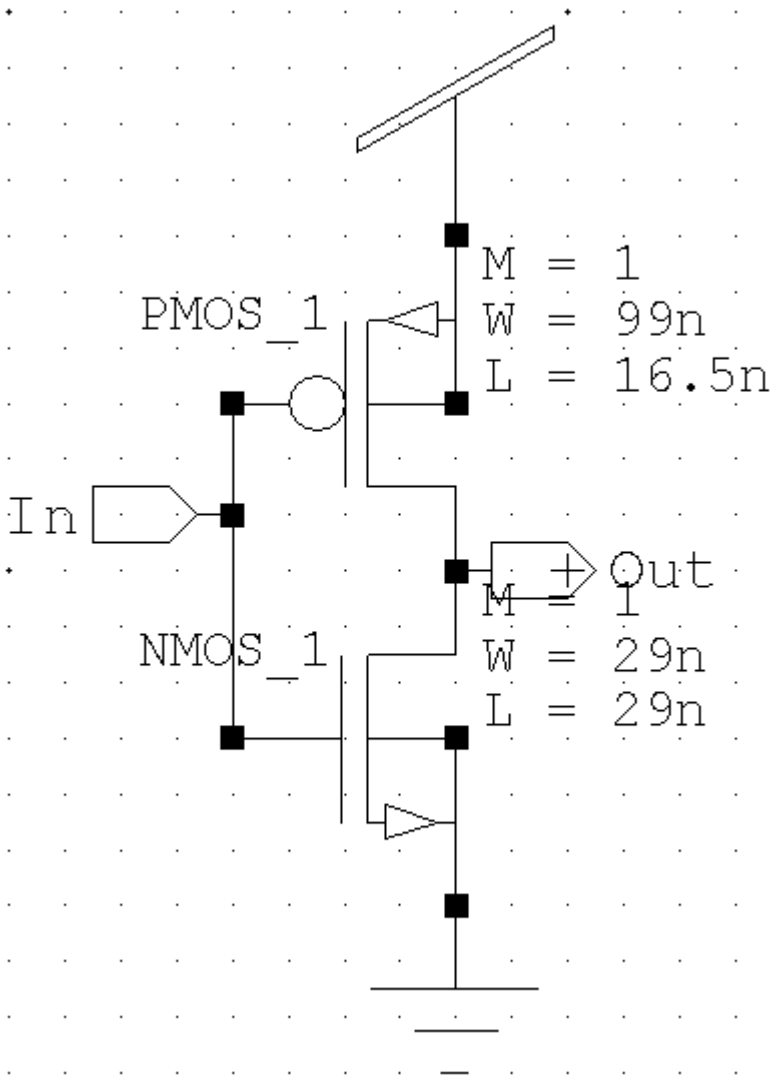


Fig 2: McCMOS inverter circuit using 16nm technology

**Table 1.2: Comparison of PDP in McCMOS inverter using different lengths & Widths**

| W & L | Power (nWatt) | Delay (n sec) | PDP ( nW-nsec) |
|---|---|---|---|
| NMOS W=25n L=25n PMOS W=25n L=16.5n | 39.05 | 0.4760 | 18.5878 |
| NMOS W=25n L=25n PMOS W=35n L=16.5n | 40.26 | 0.4060 | 16.3456 |
| NMOS W=25n L=25n PMOS W=50n L=16.5n | 41.10 | 0.3510 | 14.4261 |
| NMOS W=25n L=25n PMOS W=80n L=16.5n | 42.23 | 0.3040 | 12.8379 |
| NMOS W=33n L=33n PMOS W=80n L=16.5n | 42.27 | 0.3040 | 12.8501 |
| NMOS W=20n L=20n PMOS W=80n L=16.5n | 43.23 | 0.3030 | 13.0987 |
| NMOS W=40n L=40n PMOS W=80n L=16.5n | 42.74 | 0.3050 | 13.0357 |
| NMOS W=22n L=22n PMOS W=80n L=16.5n | 42.91 | 0.3030 | 13.0017 |
| NMOS W=28n L=28n PMOS W=80n L=16.5n | 41.92 | 0.3040 | 12.7437 |
| NMOS W=30n L=30n PMOS W=80n L=16.5n | 41.94 | 0.3040 | 12.7498 |
| NMOS W=29n L=29n PMOS W=80n L=16.5n | 41.90 | 0.3040 | 12.7376 |
| NMOS W=27n L=27n PMOS W=80n L=16.5n | 41.98 | 0.3040 | 12.7619 |
| NMOS W=28n L=28n PMOS W=99n L=16.5n | 42.38 | 0.2860 | 12.1207 |
| NMOS W=29n L=29n PMOS W=99n L=16.5n | 42.36 | 0.2860 | 12.1150 |

Fig 3 & 4 shows the circuit of CMOS and McCMOS based nand circuit.

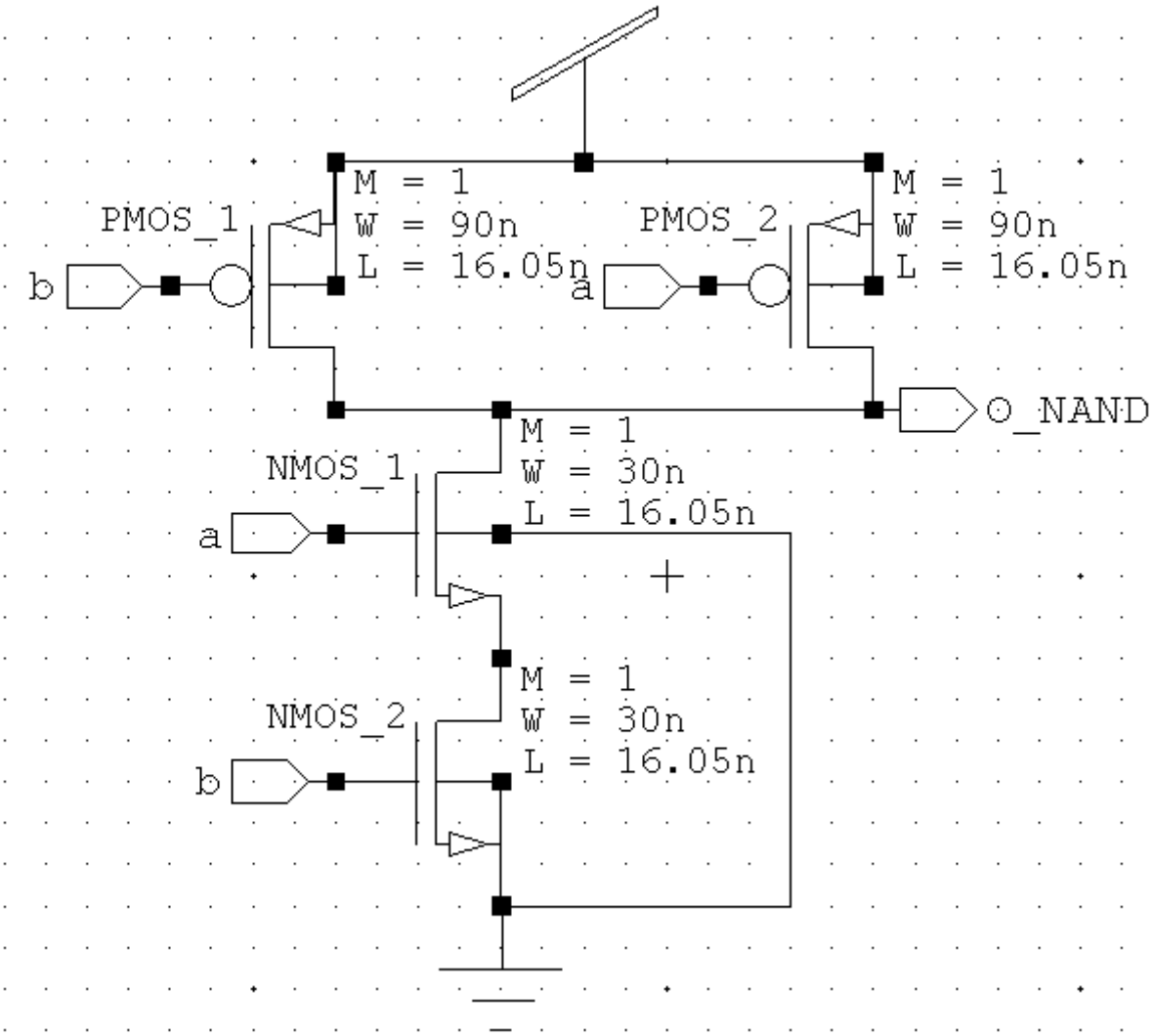


Fig 3: CMOS 2 input NAND circuit using 16nm technology

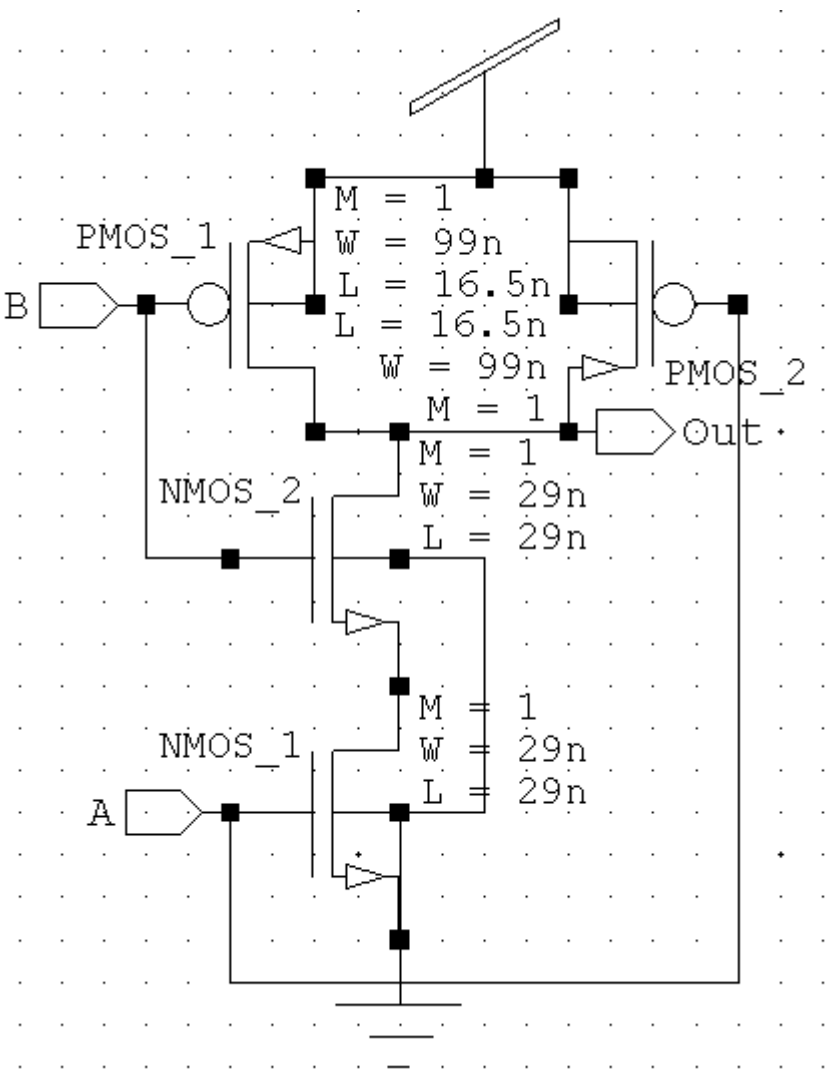


Fig 4: McCMOS 2 input NAND circuit using 16nm technology

From the table 1.3 it is clear that in McCMOS based nand circuit power & delay are much improved in comparison to its counterpart of CMOS nand circuit.
Similarly other basic component are simulated using McCMOS and CMOS and it has been verified that McCMOS based circuit has less power as well as less delay.

Table 1.3: Comparison of power & delay in CMOS & McCMOS based nand circuit.

| Technique | Length & Width | Power (nWatt) | Delay (n Sec) | PDP (atta Ws) |
|---|---|---|---|---|
| CMOS | NMOS W=30n L=16.05n PMOS W=90n L=16.05n | 92.30 | 0.40 | 37.20 |
| McCMOS | NMOS W=29n L=29n PMOS W=99n L=16.5n | 64.08 | 0.34 | 21.53 |

## 2. Vedic Mathematics

The ancient system of Vedic Mathematics was rediscovered from the Indian Sanskrit texts known as the Vedas, between 1911 and 1918 by Sri Bharati Krisna Tirthaji (1884-1960) from the Atharva Vedas. According to his research all of mathematics is based on sixteen Sutras, or word-formulas [11]. The description of urthatryakbhyam sutra and nighilum suta is given in [

### DESIGN OF THE 32x32 BIT UT MULTIPLIER

***In the design for 32x32 bit UT multiplier using McCMOS technique, we designed fundamental blocks like***

- 2x2 bit UT multiplier using McCMOS technique (fig. 5 shows schematic design & fig. 6 shows waveform)
- 4x4 bit UT multiplier using McCMOS technique (fig. 7 shows schematic design)
- 8x8 bit UT multiplier using McCMOS technique (fig. 8 shows schematic design)
- 16x16 bit UT multiplier using McCMOS technique (fig.9 shows schematic design)
- 32x32 bit UT multiplier using McCMOS technique (fig. 10 shows schematic design)

The comparison of delay, power, no of transistor used in different designed multipliers is illustrated in table 2.1.

**Table 2.1 Comparison of Designed UT Multipliers**

| Multiplier | Delay | Power | Power-delay product | No. of transistor used |
|---|---|---|---|---|
| 2x2 CMOS | 30.12 nsec | 0.7114 μW | 21.0746 nsec- μW | 60 |
| 4x4 McCMOS | 29.68 nsec | 4.97 μW | 21.42737 nsec- μW | 618 |
| 4x4 CMOS | 30.14 nsec | 4.96 μW | 147.5096 nsec- μW | 618 |
| 8x8 McCMOS | 29.67 nsec | 26.31 μW | 149.4944 nsec- μW | 3222 |
| 8x8 CMOS | 30.14 nsec | 26.92 μW | 780.6177 nsec- μW | 3222 |
| 16x16 McCMOS | 29.68 nsec | 0.108 mW | 811.3688 nsec- mW | 14382 |
| 16x16 CMOS | 30.14 nsec | 0.130 mW | 3.20544 nsec- mW | 14382 |
| 32x32 McCMOS | 29.68 nsec | 0.564 mW | 3.9182 nsec- mW | 60510 |
| 32x32 CMOS | 30.12 nsec | 0.575 mW | 16.73952 nsec- mW | 60510 |

The comparison of delay, power, no of transistor used in reported work and proposed multiplier is illustrated in table 2.2.

**Table 2.2 Comparison of UT Multiplier with Reported Work**

| UT Multiplier | Delay | Power | Power-delay product | No. of transistor used |
|---|---|---|---|---|
| Paper [2] | 59 nsec | 500 mW | 16615.2 nsec- mW | 23600 |
| Paper [3] | 15 ns | 277 mW | 1179.38 nsec- mW | 27704 |
| Paper [6] with CSA | 96.5 ns | 22.1 mW | 29.5 nsec- mW | - |
| Paper [6] with CLA | 54.1 ns | 21.8 mW | 2132.65 nsec- mW | - |
| Paper [7] | 29.67 nsec. | 0.56 mW | 17.319 nsec- mW | 60510 |
| Proposed 32x32 CMOS | 30.12 nsec | 0.575 mW | 16.73952 nsec- mW | 60510 |
| Proposed 32x32 McCMOS | 29.68 nsec | 0.564 mW | 3.9182 nsec- mW | 60510 |

Our proposed 32x32 bit multiplier using McCMOS and UT Sutra of Vedic mathematics is much far better as compared to reported work in terms of Power-Delay Product.

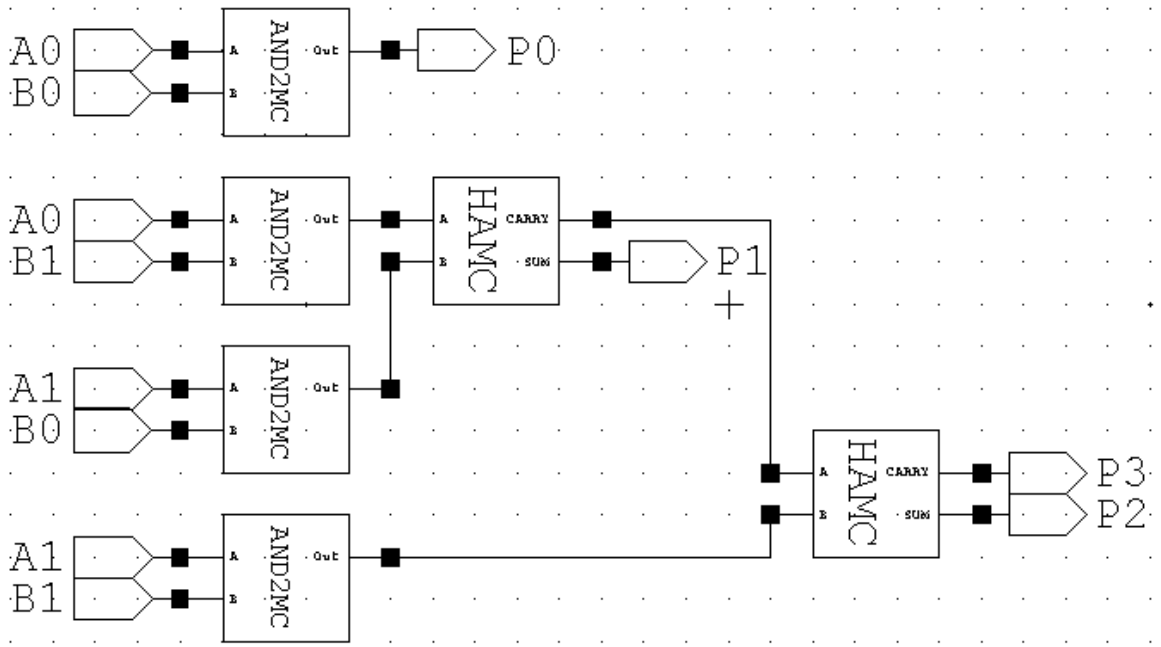


Figure5) 2 x 2 Bit Multiplier and & its symbol

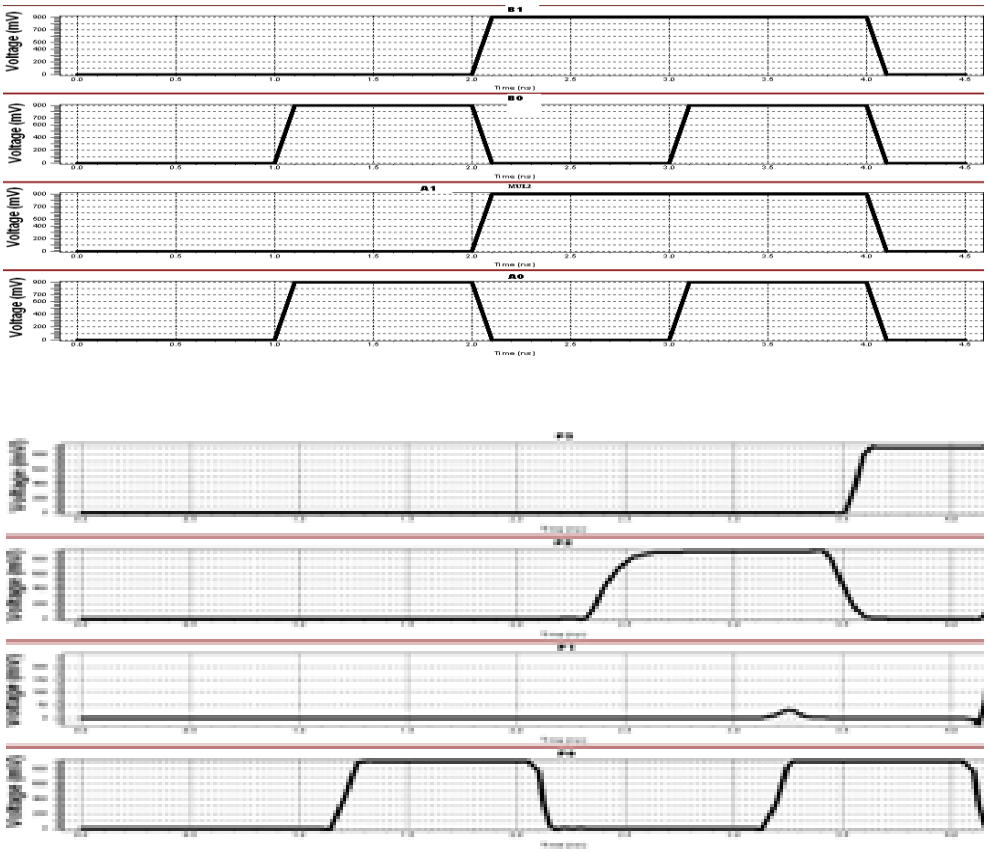


*Figure 6 Input Output waveforms of 2x2 Bit multiplier*

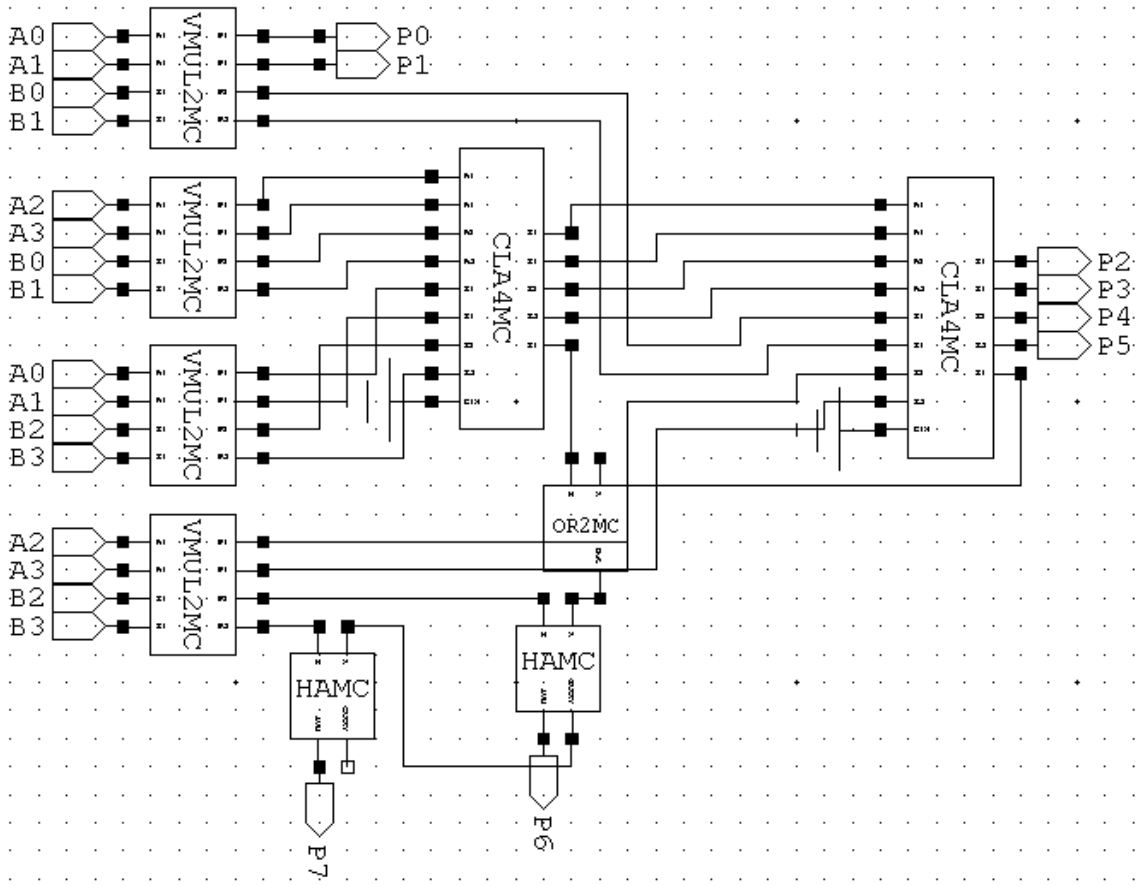


Figure7) 4 x 4 Bit Multiplier

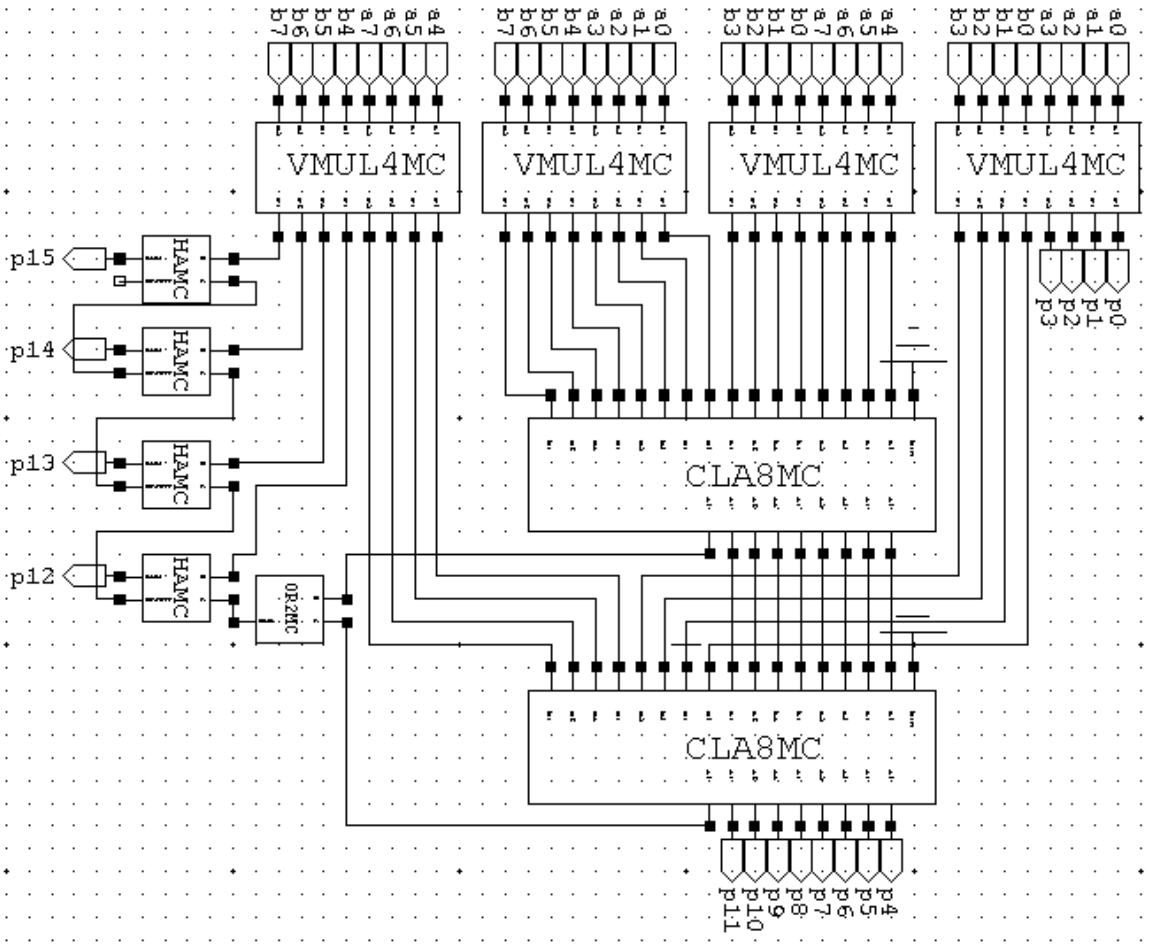


Figure8) 8 x 8 Bit Multiplier

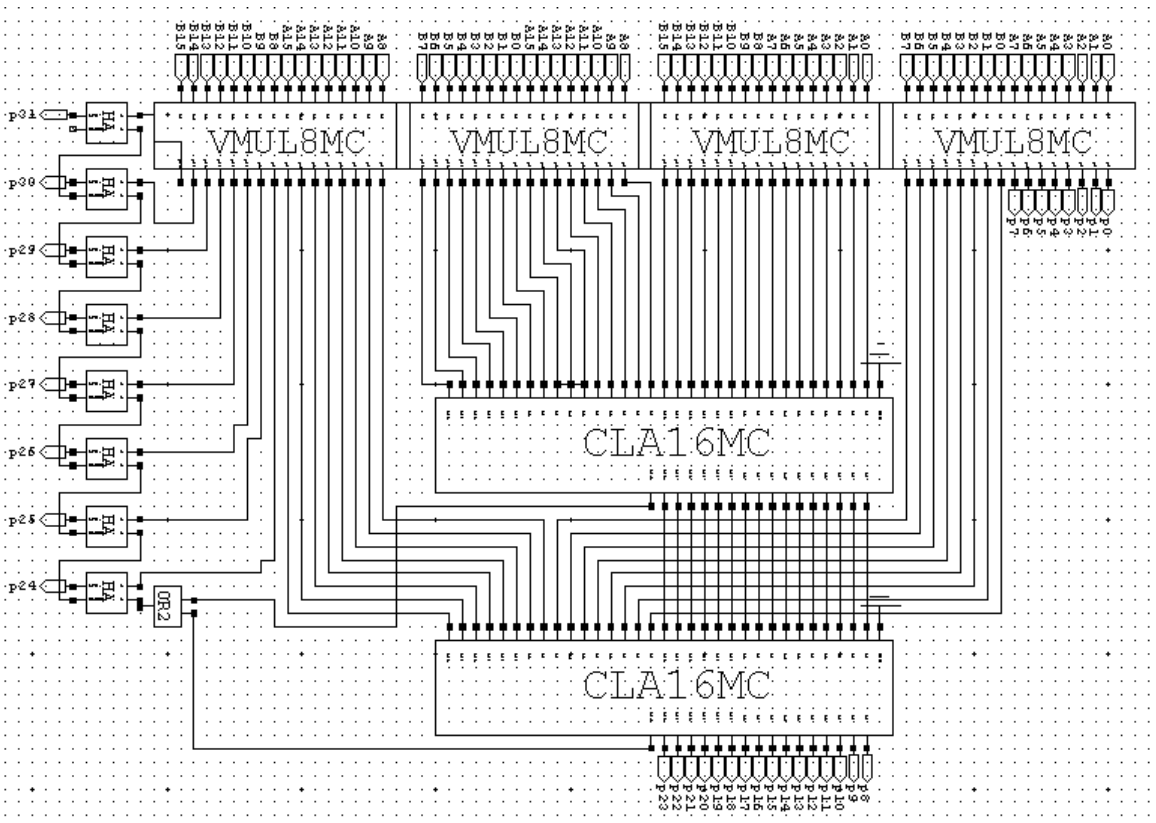


Figure9) 16 x 16 Bit Multiplier

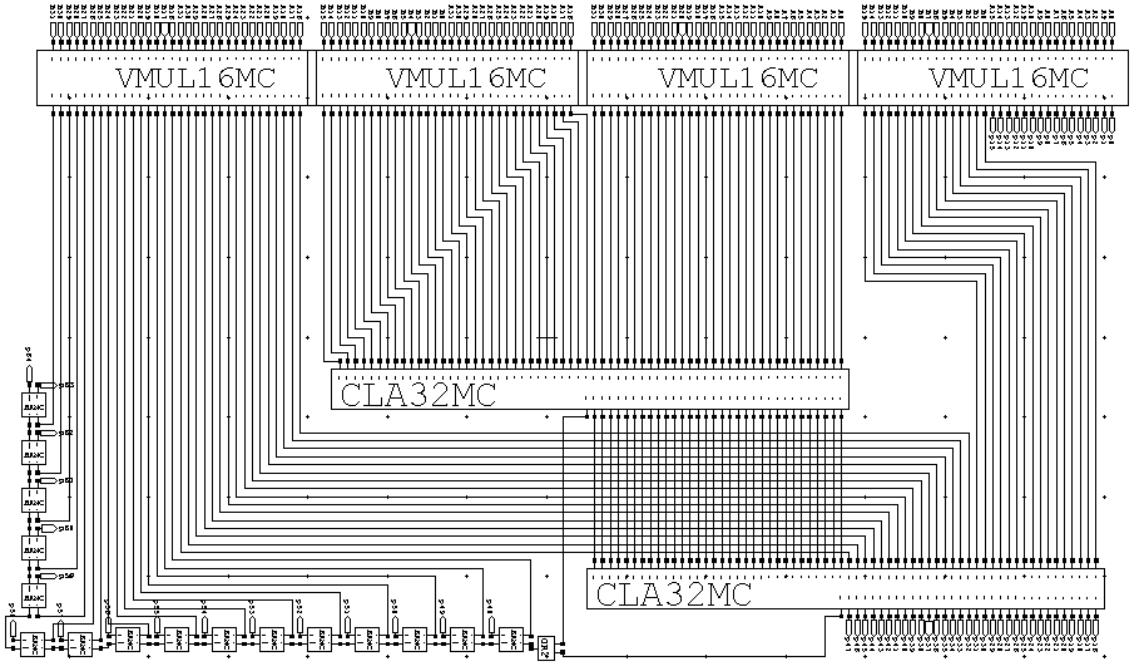


Figure10) 32 x 32 Bit Multiplier

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## 2. Design Of The 32x32 Bit Nikhilum Multiplier

***The basic structure of the Nikhilum Multiplier is shown in fig11. In the design for 32x32 bit* Nikhilum (NM) Multiplier *using McCMOS technique, we designed following fundamental blocks:***

- 2x2 bit NM multiplier using McCMOS technique (fig. 12 shows schematic design )
- 4x4 bit NM multiplier using McCMOS technique (fig. 13 shows schematic design)
- 8x8 bit NM multiplier using McCMOS technique (fig. 14 shows schematic design)
- 16x16 bit NM multiplier using McCMOS technique (fig.15 shows schematic design)
- 32x32 bit NM multiplier using McCMOS technique (fig. 16 shows schematic design)

**STEPS INVOLVED FOR MULTIPLICATION USING NIKHILUM (NM) SUTRA**

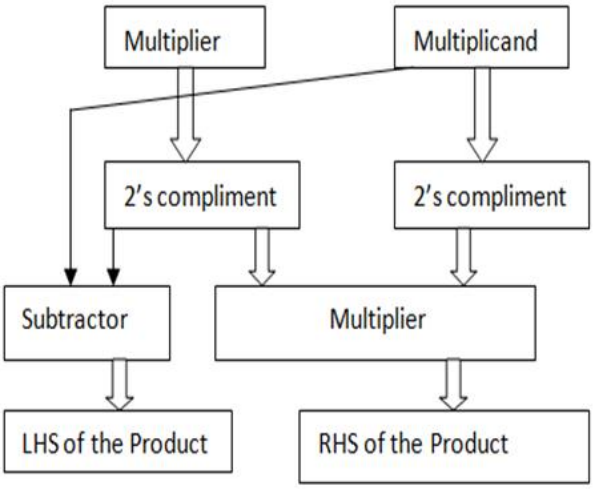


*Fig 11 Block Diagram of Nikhilum Sutra*

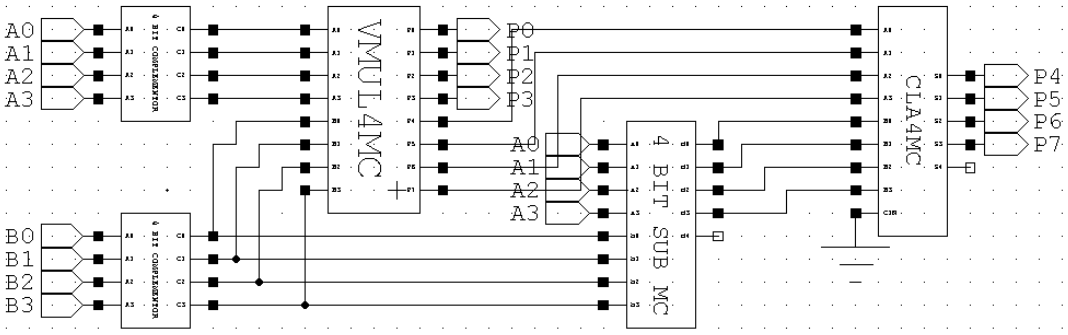


Figure12) 4 x 4 Bit Multiplier

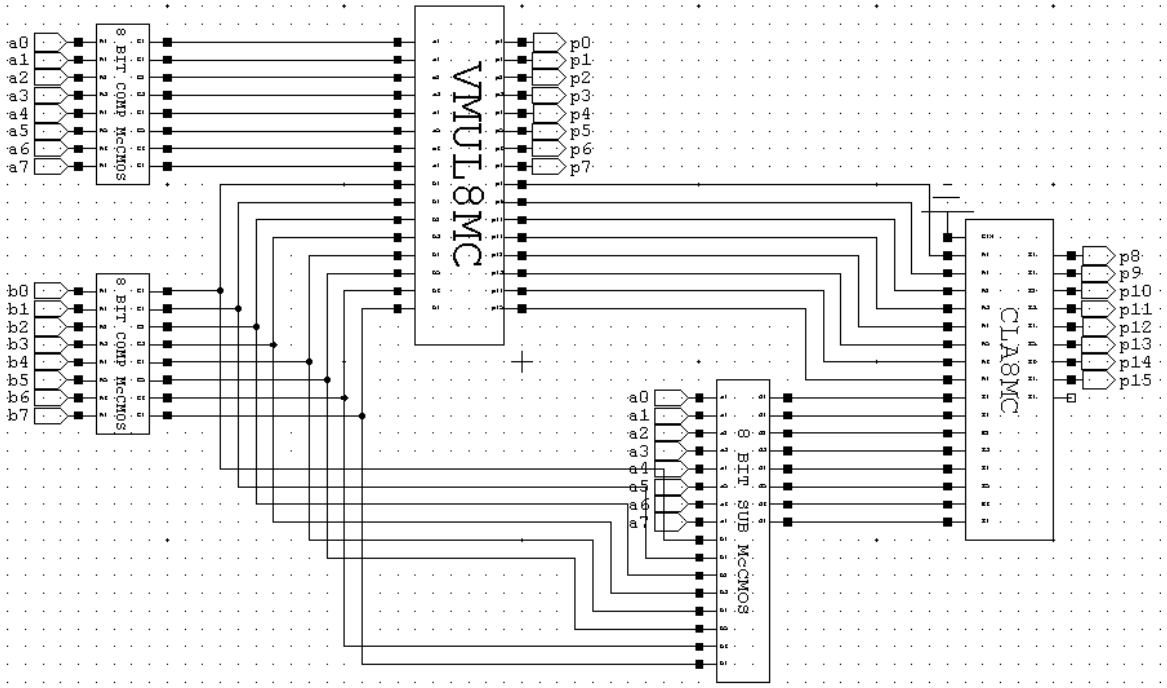


Figure13) 8 x 8 Bit Multiplier

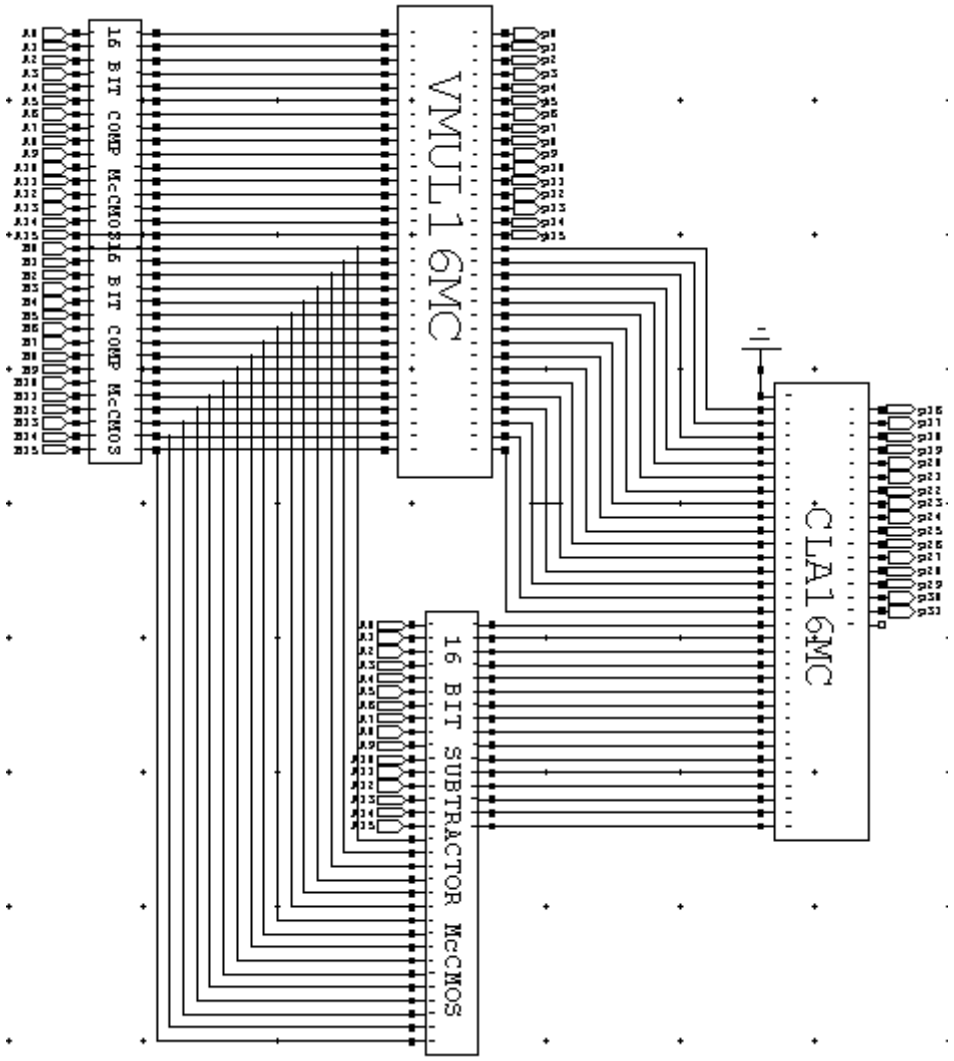


Figure14) 16 x 16 Bit Multiplier

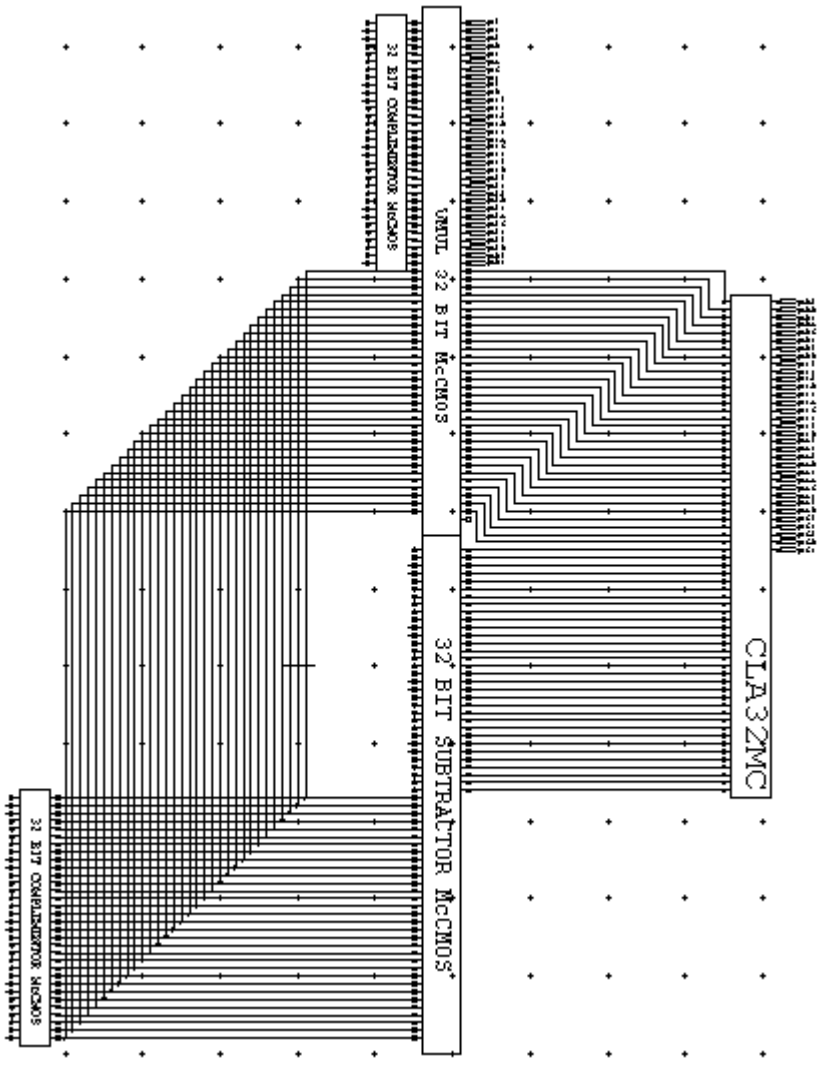


Figure 15) 32 x 32 Bit Multiplier

## 3. Conclusion

The proposed Vedic multiplier (discussed in section 3) is simulated using Tanner Tool v14.1. The Comparison between proposed multiplier and other reported multiplier is shown in table I.

**Table 4.1: Comparison of Vedic multiplier**

**POWER**

| | **UT** | **UTMcCMOS** | **NM** | **NMMcCMOS** |
|---|---|---|---|---|
| **4-BIT** | 4.96E-06 | 4.98E-06 | 8.39E-06 | 4.78E-06 |
| **8-BIT** | 2.69E-05 | 2.63E-05 | 1.94E-05 | 1.87E-05 |
| **16-BIT** | 1.30E-04 | 1.09E-04 | 1.20E-04 | 1.17E-04 |
| **32-BIT** | 5.75E-04 | 5.64E-04 | 5.60E-04 | 5.56E-04 |

**DELAY**

| | UT | UTMcCMOS | NM | NMMcCMOS |
|---|---|---|---|---|
| **4-BIT** | 3.01E-08 | 2.97E-08 | 2.90E-08 | 2.84E-08 |
| **8-BIT** | 3.01E-08 | 2.97E-08 | 2.89E-08 | 2.83E-08 |
| **16-BIT** | 3.01E-08 | 2.97E-08 | 2.88E-08 | 2.81E-08 |
| **32-BIT** | 3.01E-08 | 2.97E-08 | 2.78E-08 | 2.78E-08 |

**Table 4.2: Comparison of 32x32 bit multipliers**

| S. No. | Parameter of comparison | Paper [2] | Paper [3] | Paper [5] | Paper [6] | Nikhilum Design |
|---|---|---|---|---|---|---|
| 1 | Delay (ns) | 59 | 15 | 625.292 | 54.1 | 27.82 |
| 2 | Power (mW) | 500 | 277 | 29.34 | 21.8 | 0.556 |
| 3 | Power-Delay Product (mW-nsec) | 29500 | 4155 | 18346.067 | 1179.38 | 15.46792 |
| 4 | Transistors used | 23600 | 27704 | - | - | 64862 |

As shown in the table 4.2 our designed is much better in terms of Power dissipation. Also delay is improved. No of transistor is large but this is the sacrifice we have to pay for a less power delay product. The **99% improvement in PDP with respect to the lowest paper [6] is achieved.**

## **4.** Acknowledgement:

We sincerely thanks to the PTM website to provide the Technology file of 16 nm.

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